IN THE CLAIMS

Please amend the claims as follows:

1. (original) A Flash memory device comprising:
a memory array with a plurality of floating gate memory cells arranged in a plurality of erase blocks;
a protection register;
one or more lock bits, wherein the data contents of the protection register are rendered unwriteable by the programming of the one or more lock bits; and
a lock bit erase circuit, wherein the lock bit erase circuit is coupled to the one or more lock bits and wherein the lock bit erase circuit is operable only when the Flash memory device is in wafer form.

2. (original) The Flash memory device of claim 1, wherein the protection register contains a plurality of protection register segments, wherein each protection register segment is protected by an associated lock bit of the one or more lock bits.

3. (original) The Flash memory device of claim 1, wherein the lock bit erase circuit comprises:
a lock bit erase enable circuit; and
a floating gate erase circuit coupled to the lock bit erase enable circuit and the one or more lock bits.

4. (original) The Flash memory device of claim 3, wherein the lock bit erase enable circuit comprises:
a bond pad;
an input buffer, wherein an input of the input buffer is coupled to the bond pad;
a first pull down transistor, wherein the first pull down transistor is a weak pull down transistor;

a second pull down transistor, wherein the first and second pull down transistors are each coupled to the input of the input buffer and to ground;

an inverter coupled to an output of the input buffer and to a gate of the first pull down transistor; and

a reset signal line, wherein the reset signal line is coupled to a gate of the second pull down transistor.

5. (original) The Flash memory device of claim 4, wherein the bond pad is not coupled to an external connector when the Flash memory device is in packaged form.

6. (original) The Flash memory device of claim 1, wherein the lock bit erase circuit contains a bond pad, where the bond pad is not coupled to an external pin when the Flash memory device is in packaged form.

7. (original) A Flash memory device comprising:

a protection register having one or more protection register segments, each protection register segment having an associated lock bit, wherein the data contents of the protection register segment is unwriteable after programming the associated lock bit;

a lock bit enable circuit, wherein the lock bit enable circuit is coupled to a lock bit erase circuit which is in turn coupled to each associated lock bit of the one or more protection register segments; and

wherein the lock bit erase circuit is not coupled to an external package connector of the Flash memory device package.

8. (original) The Flash memory device of claim 7, wherein the lock bit erase circuit comprises:

a lock bit erase enable circuit; and

a floating gate erase circuit coupled to the lock bit erase enable circuit and to the one or more lock bits.

9. (original) The Flash memory device of claim 7, wherein the lock bit erase circuit contains a bond pad, where the bond pad is not coupled to an external pin when the Flash memory device is in packaged form.

10. (original) The Flash memory device of claim 7, wherein the lock bit erase circuit is adapted to allow erasure of one or more associated lock bits of the one or more protection register segments.

11. (original) A lock bit erase circuit comprising:
a bond pad;
an input buffer, wherein an input of the input buffer is coupled to the bond pad;
a first pull down transistor, wherein the first pull down transistor is a weak pull down transistor and is coupled to the input of the input buffer and to ground;
an inverter coupled to an output of the input buffer and to a gate of the first pull down transistor;
a floating gate erase circuit, wherein the floating gate erase circuit is coupled to the output of the input buffer and to one or more lock bits of a plurality of non-volatile memory cells; and
wherein the bond pad does not correspond to a standard external chip I/O (input/output) of an integrated circuit chip that incorporates the lock bit erase circuit.

12. (original) The lock bit erase circuit of claim 11, wherein the lock bit erase circuit further comprises:
a second pull down transistor, wherein the second pull down transistor is coupled to the input of the input buffer and to ground; and
a reset signal line, wherein the reset signal line is coupled to a gate of the second pull down transistor.

13. (original) The lock bit erase circuit of claim 12, wherein the lock bit erase circuit is placed in an inactive state by a transient active signal in the reset signal line, such that the inactive state is held by the active weak first pull down transistor.

14. (original) A lock bit erase enable circuit comprising:
a bond pad;
an input buffer, wherein an input of the input buffer is coupled to the bond pad and where an output of the input buffer is coupled to a floating gate erase circuit; and
wherein the bond pad does not correspond to a standard external chip I/O (input/output) of a packaged integrated circuit chip that incorporates the lock bit erase enable circuit.

15. (original) The lock bit erase enable circuit of claim 14, wherein the lock bit erase enable circuit further comprises:
a first pull down transistor, wherein the first pull down transistor is a weak pull down transistor;
a second pull down transistor, wherein the first and second pull down transistors are each coupled to the input of the input buffer and to ground;
an inverter coupled to an output of the input buffer and to a gate of the first pull down transistor; and
a reset signal line, wherein the reset signal line is coupled to a gate of the second pull down transistor.

16. (original) The lock bit erase enable circuit of claim 14, wherein the output of the input buffer is inverting.

17. (original) The lock bit erase enable circuit of claim 16, wherein the lock bit erase enable circuit further comprises:
a first pull down transistor, wherein a gate of the first pull down transistor is coupled the inverting output of the input buffer;
a second pull down transistor, wherein the first and second pull down transistors are each

coupled to a gate input of the input buffer and to ground;

a reset signal line, wherein the reset signal line is coupled to a gate of the second pull down transistor; and

a NOR gate coupled to the inverting output of the input buffer and to the reset signal line.

18. (original) A protection register comprising:

one or more protection register segments, each protection register segment having an associated lock bit; and

a lock bit erase circuit coupled to each lock bit.

19. (original) The protection register of claim 18, wherein the lock bit erase circuit further comprises:

a lock bit erase enable circuit; and

a floating gate erase circuit coupled to the lock bit erase enable circuit and to each lock bit.

20. (original) The protection register of claim 18, wherein the lock bit erase circuit is not operable when an integrated circuit having the protection register is in packaged form.

21. (original) The protection register of claim 18, wherein the protection register is incorporated in a Flash memory device.

22. (original) A system comprising:

a host coupled to a Flash memory device, wherein the Flash memory device comprises,

a memory array with a plurality of floating gate memory cells arranged in a plurality of erase blocks;

a protection register;

one or more lock bits, wherein the data contents of the protection register are rendered unwriteable by the programming of the one or more lock bits; and

a lock bit erase circuit, wherein the lock bit erase circuit is coupled to the one or more lock bits and wherein the lock bit erase circuit is inaccessible to the host.

23. (original) The system of claim 22, wherein the Flash memory device appears to the host as a rewriteable storage device.

24. (original) The system of claim 22, wherein the host is a processor.

25. (original) The system of claim 22, wherein the host is a computer system.

26. (original) The system of claim 22, wherein the lock bit erase circuit further comprises:
a lock bit erase enable circuit; and
a floating gate erase circuit, wherein the floating gate erase circuit is coupled to the lock bit erase enable circuit and the one or more lock bits.

27. (original) A Flash memory device comprising:
a memory array with a plurality of floating gate memory cells arranged in a plurality of erase blocks;
a protection register;
one or more lock bits, wherein the data contents of the protection register are rendered unwriteable by the programming of the one or more lock bits;
a bond pad;
an input buffer, wherein an input of the input buffer is coupled to the bond pad;
a first pull down transistor, wherein the first pull down transistor is a weak pull down transistor;
a second pull down transistor, wherein the first and second pull down transistors are each coupled to the input of the input buffer and to ground;
an inverter coupled to an output of the input buffer and to a gate of the first pull down transistor;
a reset signal line, wherein the reset signal line is coupled to a gate of the second pull

down transistor;

a lock bit erase circuit, wherein the lock bit erase circuit is coupled to the output of the input buffer and to the one or more lock bits; and

a package containing the Flash memory device, wherein the bond pad is not coupled to an external connector of the package.

28. (original) The Flash memory device of claim 27, wherein the protection register has a plurality of protection register segments, such that each protection register segment is associated with a lock bit.

29. (original) The Flash memory device of claim 28, wherein each protection register segment contains 64 bits of data.

30. (original) The Flash memory device of claim 27, wherein the protection register has 128 bits of data.

31. (original) The Flash memory device of claim 27, wherein the protection register is mapped into an address range of the memory array.

32. (original) A method of operating a Flash memory device comprising:

enabling erasure of one or more lock bits associated with a protection register when the Flash memory device is in wafer form; and

disabling erasure of the one or more lock bits when the Flash memory device is in packaged form.

33. (original) The method of claim 32, wherein enabling erasure further comprises enabling erasure by forming a lock bit erase circuit on the Flash memory device.

34. (original) The method of claim 32, wherein enabling erasure further comprises enabling erasure by coupling a chip test probe to a bond pad of a lock bit erase circuit when the Flash memory is in wafer form.

35. (original) The method of claim 32, wherein disabling erasure further comprises disabling erasure by not coupling a bond pad of a lock bit erase circuit to an external connector of the Flash memory device in packaged form.

36. (Currently Amended) A method of erase enabling the lock bits of a protection register comprising:

forming a floating gate erase circuit coupled to one or more lock bits of a protection register; and

forming a lock bit erase enable circuit coupled to the floating gate erase circuit, wherein the ~~erase block~~ lock bit erase enable circuit is operable only when an integrated circuit containing the protection register is in wafer form.

37. (Currently Amended) The method of claim 36, wherein forming the ~~erase block~~ lock bit erase enable circuit further comprises:

forming a bond pad;

forming an input buffer, wherein an input of the input buffer is coupled to the bond pad and where an output of the input buffer is coupled to ~~a~~ the floating gate erase circuit.

38. (original) The method of claim 37, wherein forming the lock bit erase enable circuit further comprises:

forming a first pull down transistor, wherein the first pull down transistor is a weak pull down transistor;

forming a second pull down transistor, wherein the first and second pull down transistors are each coupled to the input of the input buffer and to ground;

forming an inverter coupled to an output of the input buffer and to a gate of the first pull

down transistor; and

forming a reset signal line, wherein the reset signal line is coupled to a gate of the second pull down transistor.

39. (original) The method of claim 37, wherein the output of the input buffer is inverting.

40. (original) The method of claim 39, wherein forming the lock bit erase enable circuit further comprises:

forming a first pull down transistor, wherein a gate of the first pull down transistor is coupled the inverting output of the input buffer;

forming a second pull down transistor, wherein the first and second pull down transistors are each coupled to a gate input of the input buffer and to ground;

forming a reset signal line, wherein the reset signal line is coupled to a gate of the second pull down transistor; and

forming a NOR gate coupled to the inverting output of the input buffer and to the reset signal line.

41. (original) A method of erase disabling the lock bits of a floating gate register comprising:

enabling lock bit erase by coupling to a lock bit erase circuit with a test card probe when an integrated circuit containing the floating gate register is in wafer form; and

disabling the lock bit erase circuit when the integrated circuit containing the floating gate register is in packaged form.

42. (original) The method of claim 41, wherein disabling the lock bit erase circuit when the integrated circuit containing the floating gate register is in packaged form further comprises disabling the lock bit erase circuit when the integrated circuit containing the floating gate register is in packaged form by not coupling an external connector to a bond pad of the lock bit erase circuit.

43. (original) The method of claim 41, wherein coupling to a lock bit erase circuit when an integrated circuit containing the floating gate register is in wafer form further comprises

coupling to a lock bit erase circuit with a test card probe when the integrated circuit containing the floating gate register is in wafer form.

44. (original) A method of making a Flash memory device comprising:
forming a memory array containing a plurality of floating gate memory cells arranged in a plurality of erase blocks;
forming protection register and one or more associated lock bits;
forming a floating gate erase circuit coupled to the one or more lock bits of the protection register; and
forming a lock bit erase enable circuit coupled to the floating gate erase circuit, wherein the erase block enable circuit is operable only when the Flash memory device is in wafer form.

45. (original) A method of manufacturing a Flash memory device comprising:
programming a lock bit by applying a control signal to an input; and
packaging the Flash memory device such that the input is inaccessible.

46. (original) The method of claim 45, further comprising:
reprogramming the lock bit prior to packaging.

47. (original) The method of claim 46, wherein reprogramming the lock bit prior to packaging further comprises erasing the lock bit prior to packaging.